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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/321,605	05/28/1999	NAOYA SASHIDA	990535	6725

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EXAMINER	
CHEN, JACK S J	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 11/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/321,605	SASHIDA ET AL.	
	Examiner	Art Unit	
	Jack Chen	2813	

-- Th MAILING DATE of this communication appears on th cover sh et with th correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 August 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) *4,5 and 17-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3, 6-16, 21-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 1-3, 9, 11-16, 21-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Mochizuki et al., U.S./5,990,507.

Mochizuki et al. discloses a method of forming a semiconductor device, which comprises forming a couple of impurity diffusion layers S/D in a substrate; forming a first insulating film 10 (figs. 21 or 22, which is SiO2) covering the substrate; forming a lower electrode 17 (Pt) of a capacitor on the first insulating film; forming an oxide dielectric film 18 (PZT) of the capacitor on

the lower electrode; forming an upper electrode 19 (Pt) of the capacitor on the oxide dielectric film; forming a second insulating film 13 (SiO2) for covering the capacitor; forming a first opening for electrically connecting the impurity diffusion layer and a second opening on the upper electrode in the first and second insulating films, by etching a part of the second insulating film and a part of the first insulating film (figs. 21 or 22); forming a metal 111 (titanium nitride, figs. 21or 22) film on the second insulating film for connecting electrically the impurity diffusion layer via the first opening and the upper electrode via the second opening; forming a local interconnection in a range which pass through the first opening and the second opening and contains at least a region where the upper electrode contacts the oxide dielectric film (see figs. 21 or 22; layer 111, which shows the local interconnection in a range which pass through the first opening and the second opening, and contains at least a region where the upper electrode contacts the oxide dielectric film, 18 contacts with 19), by patterning the metal film, or forming a local interconnection covering an entire portion of the upper electrode with an area which is larger than an area where the upper electrode contacts with the oxide dielectric film in a plan view (i.e., at a plane parallel to the drawing figures, i.e., see figs.17, 19, 20, 21, 22, 23), the entire portion being with respect to a width and a length of the upper electrode (i.e., see figs.17, 19, 20, 21, 22, 23), in a range which passes through the first opening and the second opening, by patterning the metal film 111 fig. 21 or 22, also see fig. 19, layers 22/11' or 36/11' or fig. 20, layer 22, or fig. 21, layers 111/22/11' or fig. 22, layers 22/11' or fig. 23, layers 11/22); wherein the local interconnection is a blocking layer for preventing a diffusion of a redundant to the oxide dielectric film (since the same

material (TiN) is used for the metal layer, which is the same as applicant's claimed invention); and forming a third insulating film 30 for covering the local interconnection; forming a third opening for electrically connecting to the other of the couple of impurity diffusion layers (fig. 21), by etching a part of the third insulating film; and forming a wiring 38/112 electrically connecting to the other of the couple of impurity diffusion layers, the wiring composed from multi-layer films (for example, Al/TiN/Ti), the wiring having lower resistance than the local interconnection, see figs. 1-28, cols. 1-40.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 6-8, 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mochizuki et al., U.S./5,990,507 in view of Kawai et al., U.S./6,022,774.

Mochizuki et al. disclosed above; however, Mochizuki et al. does not explicitly shows the second or third insulating films (SiO2) are formed by using silane; and the second insulating film (SiO2) is formed by using TEOS and carrying out a step of oxygen-annealing after forming the second opening.

Kawai et al. discloses a method of forming a semiconductor device, which comprises forming an impurity diffusion layer in a substrate; forming a first insulating film covering the substrate; forming a lower electrode 31 of a capacitor on the first insulating film; forming an oxide dielectric film 32 of the capacitor on the lower electrode; forming an upper electrode 33 of the capacitor on the oxide dielectric film; forming a second insulating film 34 (SiO2, by using TEOS or silane) for covering the capacitor; forming a first opening which exposes the impurity diffusion layer and a second opening which exposes the upper electrode in the first and second insulating films, by etching a part of the second insulating film and a part of the first insulating film (figs. 2G); forming a metal film (titanium nitride, which is the same as applicant's claimed invention) on the second insulating film via the first opening and the upper electrode via the second opening, forming a local interconnection covering an entire portion of the upper electrode with an area which is larger than an area where the upper electrode contacts with the oxide dielectric film in a plan view (i.e., at a plane parallel to the drawing figures, i.e., figs. 1F, 2H), wherein the metal is a blocking layer for preventing a diffusion of a redundant to the oxide dielectric film; and carrying out various steps of oxygen annealing after each the etching steps such will improve the oxide dielectric layer, see fig. 1 A-2H and cols. 1-8.

Therefore, the subject matter as a whole would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify the standard process of Mochizuki et al. by using TEOS or silane to form the second insulating film (SiO2) and carrying

out a step of oxygen-annealing after forming the second opening as taught by Kawai et al. in order to improve the oxide dielectric layer characteristics.

Response to Arguments

5. Applicant's arguments filed August 21, 2003 have been fully considered but they are not persuasive.

Applicant argues that the prior art (Mochizuki et al.) does not show forming a local interconnection covering an entire portion of the upper electrode with an area which is larger than an area where the upper electrode contacts with the oxide dielectric film in a plan view, the entire portion being with respect to a width and a length of the upper electrode. The Examiner disagrees. First, applicant fails to defined "plan view" i.e., which plan? In this case, Mochizuki et al. clearly shows forming a local interconnection covering an entire portion of the upper electrode with an area which is larger than an area where the upper electrode contacts with the oxide dielectric film in a plan view (i.e., ***at a plane parallel to the drawing figures***, i.e., see figs.17, 19, 20, 21, 22, 23), the entire portion being with respect to a width (vertical direction) and a length (horizontal direction) of the upper electrode (i.e., see figs.17, 19, 20, 21, 22, 23). Further in this regard, the claimed feature (9a) of the drawing (fig. 1F) of the instant application is the same as the figs. 17, 19-23 (elements 11'/22/36) as shown in the prior art. Applicant further argues that fig. 8 of the prior art does not show local interconnection covering an entire portion of the upper electrode with an area which is larger than an area where the upper electrode contacts with the

oxide dielectric film in a plan view, the entire portion being with respect to a width and a length of the upper electrode; the Examiner agrees with the applicant, however, it is noted that this particular figure is only one of the disclosed embodiments (which drawn to figs. 9-12, where the local interconnection 21/22 does not cover the entire portion of the upper electrode 19).

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jack Chen whose telephone number is (703) 308-5838. The examiner can normally be reached on Monday-Friday (alternate Monday off) from 8:30 am to 6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached on (703)308-4940. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Jack Chen

Primary Examiner

November 1, 2003